

EXHIBIT 14

EXHIBIT 5

**IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
MIDLAND-ODESSA DIVISION**

REDSTONE LOGICS LLC,) MO:24-CV-00028-ADA-DTG
)
Plaintiff,)
)
v.) WACO, TEXAS
)
NXP SEMICONDUCTORS N.V., NXP B.V.,)
NXP USA, INC.,)
)
Defendants.) FEBRUARY 19, 2025

REDSTONE LOGICS LLC,) MO:24-CV-00029-ADA-DTG
)
Plaintiff,)
)
v.) WACO, TEXAS
)
MEDIATEK, INC., MEDIATEK USA, INC.,)
)
Defendants.) FEBRUARY 19, 2025

TRANSCRIPT OF CLAIMS CONSTRUCTION HEARING
BEFORE THE HONORABLE RONALD C. GRIFFIN

FOR THE PLAINTIFF: CHRISTIAN W. CONKLE
QI (PETER) TONG
JOSHUA SCHEUFLE
RUSS AUGUST & KABAT
12424 WILSHIRE BOULEVARD, 12TH FLOOR
LOS ANGELES, CALIFORNIA 90025

FOR THE DEFENDANTS: ERIC CONLEY GREEN
BRETT A. MCKEAN
NORTON ROSE FULBRIGHT US LLP
98 SAN JACINTO BOULEVARD, SUITE 1100
AUSTIN, TEXAS 78701

RICHARD S. ZEMBEK
NORTON ROSE FULBRIGHT US LLP
1550 LAMAR STREET, SUITE 2000
HOUSTON, TEXAS 77010

1 clarification on that with this definition so that the
2 parties will know how to frame both invalidity and
3 infringement briefs. So, with that, Mr. Scheufler, are
4 you handling this?

5 MR. SCHEUFLER: Yes, Your Honor.

6 THE COURT: All right. Very good. Whenever
7 you're ready.

8 MR. SCHEUFLER: All right. Well, I'd like to
9 jump right in it, then. You asked about whether a single
10 clock source -- whether we would need a single clock
11 source or multiple clock sources, and that being the
12 maybe rub. And I think the claim language itself
13 provides us the answer.

14 The claim language says that first clock signal
15 is independent from the second clock signal. Not that
16 they're independent from a common source, but it is with
17 respect to each other.

18 So looking at what NXP has argued, I call this
19 the mathematical version of "independence." The purely
20 mathematical approach is to say that, well, if any part
21 of a component of your final outcome is common, then they
22 are not independent.

23 But looking at this example, I believe it's
24 just fundamentally wrong. So in this example we have a
25 frequency F coming in to two handlers, the top being

1 shown as X divided by 2, the bottom being X divided by 4.

2 In Kim, for example, these are PLLs. PLLs are
3 not static like this. They are in fact changing. So
4 it's not just X over 4. It's going to be X over Y, X
5 over Z, such that these can change what they're doing to
6 the incoming frequency independently. The Y does not
7 depend on what you do with the Z, and vice versa. So
8 your outcome is going to be the frequency divided by Y
9 frequency divided by Z. And those can be changed
10 completely independently without regard to what you're
11 doing with the other.

12 You can have a common incoming. Let's just
13 give an example and say it's 8. You can choose Y to be 2
14 and Z to also be 2, or you could choose Z to be 4 and
15 keep Y as 2. They can change completely independently of
16 one another, and your end signal is going to be whatever
17 you want it to be, completely irrespective of what you
18 have as your incoming signal F.

19 Now if we can jump back for a moment, jump back
20 to slide 6, and we can talk about what the applicant was
21 doing with this amendment. Defendants agree that -- or
22 at least NXP agrees with this amendment, that the
23 applicant added several additional limitations. It took
24 what was just the first output clock signal and the
25 second output clock -- or second clock signal and made it

1 the first output clock signal and added a phase lock
2 loop, first and second phase lock loop and a first and
3 second clock signal, as input to those phase lock loops,
4 and set those first and second clock signals as inputs to
5 be independent.

6 Now, why did the applicant do it? Turning to
7 slide 7, here we have the interview with the examiner.
8 The applicant is talking about how the clock signals 1
9 through 3 of its figure are different, independent clock
10 signals going into the PLLs compared with *Jacobowitz'*
11 disclosure of just a single signal, the V sub R, going
12 into its local oscillators.

13 The examiner agreed that, yes, those things are
14 different but it's irrelevant. It's irrelevant because
15 the broadest reasonable interpretation of the claims as
16 they were at the time, i.e., just that the first set of
17 processor cores is configured to dynamically receive a
18 first clock signal with no regard to PLLs or whether that
19 clock signal is an input to the PLL or an output to the
20 PLL, covers not V sub R, but V sub 1 and V sub 0.

21 So what -- what all does that add. Well, let's
22 look at figure - the patent's figure 3 on the next slide,
23 slide 8. So I have color coded things here to hopefully
24 make it a little easier to understand what all is now
25 added and claimed. So we claim an output clock signal.

REPORTER'S CERTIFICATE

I, Arlinda Rodriguez, do hereby certify that the foregoing was transcribed from an electronic recording made at the time of the aforesaid proceedings and is a correct transcript, to the best of my ability, made from the proceedings in the above-entitled matter, and that the transcript fees and format comply with those prescribed by the Court and Judicial Conference of the United States.

/S/ Arlinda Rodriguez

April 1, 2025

ARLINDA RODRIGUEZ

DATE